LM5115A Evaluation Board

National Semiconductor
Application Note 1542
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Introduction

The LM5115A/LM5025A evaluation board provides a typical application circuit of a secondary side post regulated (SSPR) output from an existing Active Clamp Forward converter. This SSPR output voltage tracks the output voltage of the active clamp forward converter during Power-Up/Power-Down. Information on the LM5025A active clamp evaluation board can be found in Application Note AN-1345. Note that other types of isolated power converters (e.g. push-pull, half-bridge, and full-bridge) can be used in the place of the LM5025A active clamp forward converter to drive the LM5115A AC evaluation board.

The evaluation board specifications are:

- Input voltage: 36V to 72V, 48V nominal on LM5025A
- Output voltage Main: 3.3V nominal
- Output current Main: 0 to 30A
- Current limit Main: ≅30A
- Output voltage Secondary: 2.5V
- Output current Secondary: 0 to 9A
- Current limit Secondary: ≅10A
- Measured efficiency on secondary only: 98% at 36V, Iload = 1A, 93% at 48V, Iload = 4A
- Load regulation: 2mV change from 1A-7A, 36V < Vin < 72V
- Size: 2.175 x 1.125 x 0.0375 in.

The printed circuit board consists of 4 layers of 2 oz copper on FR4 material, with a thickness of 0.050 in. It is designed for continuous operation at rated load with a minimum airflow of 200 LFPM.

Theory of Operation

The LM5115A controller contains all of the features necessary to produce multiple tracking outputs using the Secondary Side Post Regulation (SSPR) technique. The SSPR technique develops a highly efficient and well regulated auxiliary output from the secondary side switching waveform of an isolated power converter.

Synchronization of the LM5115A comes from the main pulsed signal of the transformer secondary winding. Resistors R2 and R4 sense the pulsing signal to form an internal synchronization current signal. The LM5115A controls the buck power stage with leading edge pulse width modulation (PWM). Leading edge modulation delays the rising edge of the main pulsed signal by holding off the LM5115A high-side gate driver therefore, establishing the required voltage*seconds to regulate the SSPR output. Representative waveforms are shown in Figure 8.

Bias to the part comes from a rectified pulse signal. Note that the pulse signals vary from 6Vpp to 12Vpp, with Vin varying from 36V to 72V, respectively. Therefore, the Vcc regulator will not regulate at 7V until the peak to peak voltage is slightly higher than 7.5V (accounting for the diode drop to the bias). This set up shows that even with unregulated Vcc the LM5115A is still capable of providing the secondary voltage of 2.5V from the main 3.3V. Adaptive deadtime control delays the top and bottom drivers to avoid shoot through currents (Figure 9 & 10).

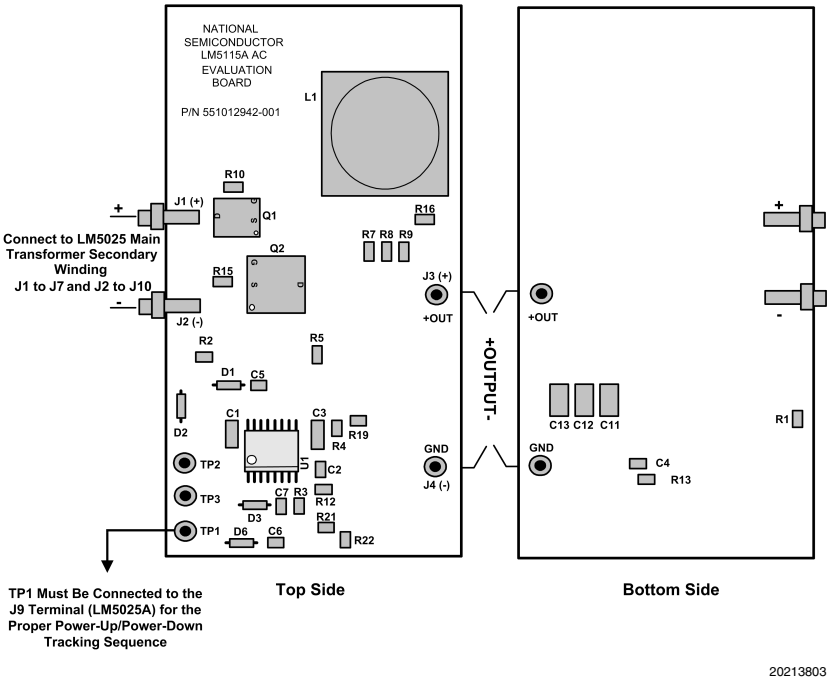

FIGURE 1. LM5115A Evaluation Board

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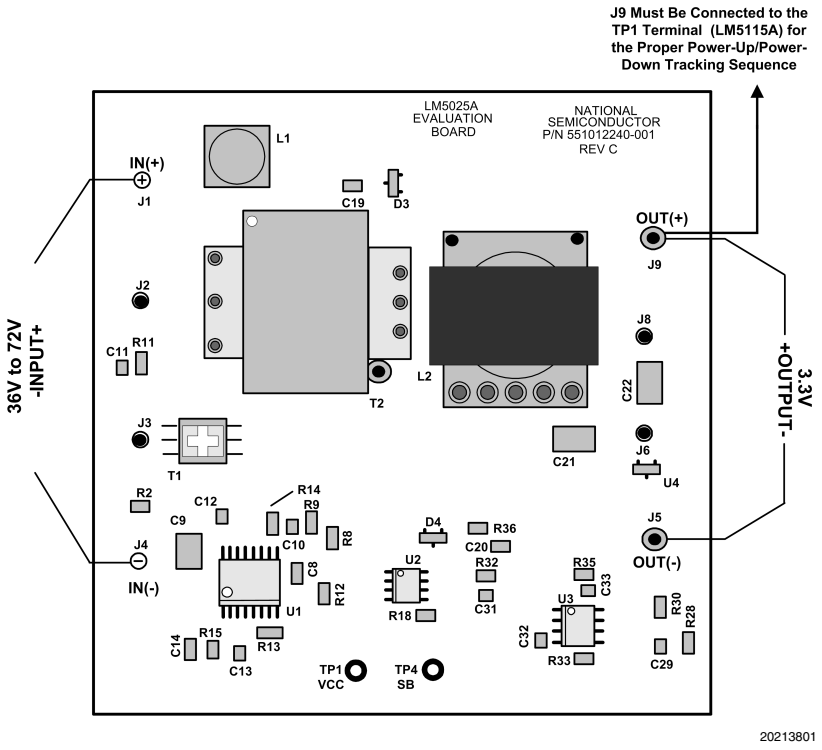


FIGURE 2. LM5025A Evaluation Board Top Side

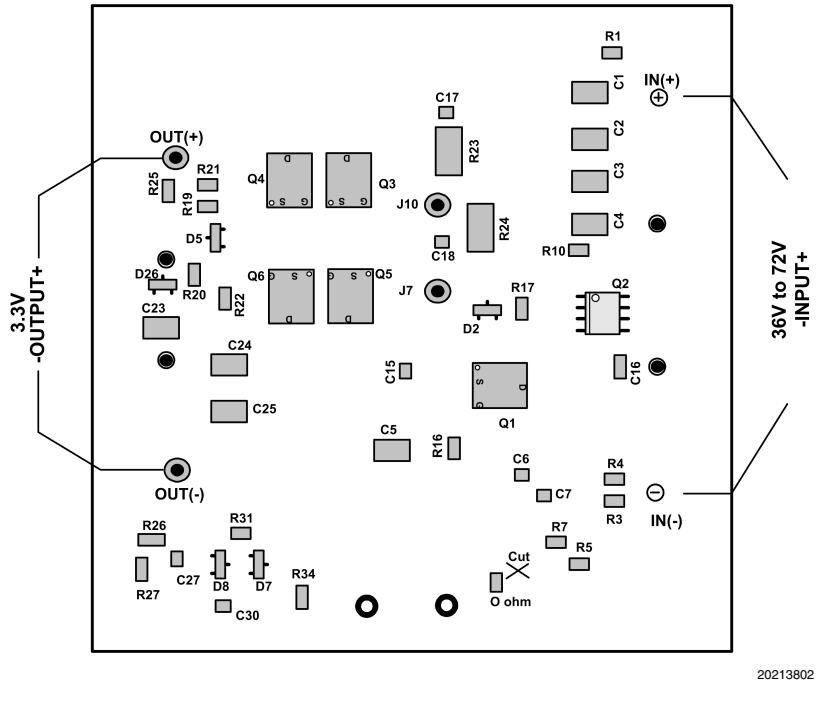


FIGURE 3. LM5025A Evaluation Board Bottom Side

Board Layout and Probing

Figures 1-3 show the board layout, main components, and critical probe points for testing the LM5115A AC evaluation board in conjunction with the LM5025A board. The following notes should be considered prior to applying power to the board:

1. Main input power (36V to 72V) is applied to points J1 and J4 of the LM5025A board, connected to VIN and GND respectively.
2. The main current carrying components (LM5115A board: L1, Q1, and Q2; LM5025A board L2, Q3-Q6) will be hot to the touch at maximum load current. USE CAUTION. When operating at load currents in excess of 5A the use of a fan to provide forced air flow **IS NECESSARY**.
3. The diameter and length of the wire used to connect the load is important. To ensure that there is not a significant voltage drop in the wires, a minimum of 14 gauge wire is recommended.

Board Connections/Start-Up

The input power connections are made to terminals J1 (+) and J4 (-) of the LM5025A evaluation board. The input source must be capable of supplying the load on both the output of the LM5025A board and LM5115A board. The input to the LM5115A is supplied by the secondary winding of the LM5025A board. J7 (LM5025A) connects to J1 (LM5115A) and J10 (LM5025A) connects to J2 (LM5115A) (see Figure 1-3). The main load is connected to terminals J9 (+) and J5 (-) for the LM5025A. Terminals J3 (+) and J4 (-) are the load connections for the LM5115A. Before start-up, a voltmeter should be connected to the input terminals and to the output terminals. The input current should be monitored with an ammeter or a current probe.

Note that for the proper Power-Up/Power-Down tracking sequence, the J9(+) terminal, the LM5025A Vout (+) terminal, must be connected to the TP1 terminal, the LM5115A TRACK post, (see Figure 1-3). To disable the tracking feature R21 and R22 should be removed from the LM5115A evaluation board and the soft start capacitor C2 (.1µF) should be added to the board.

Performance LM5115A Secondary Side Post Regulator

Performance of the LM5115A evaluation board can be seen in the following figures:

1. Power Conversion Efficiency (Figure 4 & 5)
2. Load Regulation (Figure 6)
3. Secondary Closed Loop Frequency Response (Figure 7)
4. Representative Waveforms (Figure 8)
5. Gate Delays (Figure 9 & 10)
6. Short Circuit Response (Figure 11)
7. Step Load Response (Figure 12 & 13)
8. Power-up/Power-Down Tracking (Figure 14 &15)
9. Output Voltage Ripple (Figure 16)

V_{CC}

The LM5115A produces a LDO 7V regulated output (VCC) that can supply up to 40mA of DC current. The VCC regulator supplies power for the high current gate drive for the low-side MOSFET and the bootstrap capacitor of the high side MOSFET driver.

Tracking/Soft-Start

Connecting the J9(+) terminal to the TP1 terminal will force the output voltage of the LM5115A evaluation board to track the master power supply output voltage (the LM5025A evaluation board output voltage) at Power-Up/Power-Down. TP1 is connected through a resistor divider (R21& R22) to the LM5115A TRACK pin (Figure 18). Therefore, the output voltage slew rate of the LM5115A evaluation board will be controlled by the master supply at Start-Up/Shut-Down. The LM5115A evaluation board is configured to demonstrate that the LM5115A can be used in applications which require precise sequencing. To disable the Tracking feature, R21 and R22 should be removed from the LM5115A evaluation board and the soft start capacitor C2 (.1uF) should be added to the board. For more information regarding the Tracking feature please refer to the LM5115A datasheet.

Current Limit Operation

The inductor current is sensed through resistor R8. The resistor value is designed for a current limit of ~10A. The LM5115A has two current limit amplifiers that monitor the sensed current signal across R8. The common output port of these current limit amplifiers,the CO pin, is connected to the COMP pin through a diode (D3). The slow current limit amplifier provides constant current operation at the desired current limit set point. The fast current limit amplifier provides protection against fast over-current conditions. During normal operation, the voltage error amplifier controls the COMP pin voltage which adjusts the PWM duty cycle. However when the current sense input voltage exceeds 45mV, the slow current limit amplifier gradually pulls down on COMP through the CO pin. Pulling COMP low reduces the operating duty cycle. By controlling the operating duty cycle, the slow current limit amplifier will force constant current operation at the desired current limit set point. R19 and C6 are connected in series from the CO Pin to ground to provide adequate control loop compensation for the slow current limit (Figure 18). The desired current limit set point, ILimit, can be programmed by selecting the proper current sense resistor, R_{SENSE},using the following equation:

$$R_{SENSE} = 0.045\ V/\ ILimit$$

In the event that the current sense input voltage exceeds 60mV, the fast current limit amplifier will pull down hard on COMP through the CO pin.Therefore, the PWM comparator will inhibit output pulses. Once the fault condition is removed, the fast current limit amplifier will release COMP. Therefore, the switching will resume .

The current limit scheme explained above provides an average current limit mode of operation. The LM5115A evaluation board can be also configured for cycle by cycle current limiting. In this mode, the CO pin will pull the SYNC pin to ground through the diode D6 once the voltage across the sense resistor, R8, exceeds 45mV. Therefore the high-side MOSFET will turn-off instantaneously to terminate the on-pulse. The cycle by cycle current limiting should only be used if the master power supply uses a voltage mode (or voltage mode with feed forward) control loop scheme. If cycle by cycle current limiting is used while the master power supply is utilizing current mode control scheme an oscillation will occur. To configure the LM5115A evaluation board for cycle by cycle current limiting, C9, R19, D3 have to be removed and D6 has to be added to the board.

In cases where a noisy current sense is present, adding a low pass filter to the input of CS and VOUT can help restore a

cleaner waveform (*Figure 17* , R16 and C10). Care must be taken not to have a large RC time constant to avoid instability.

Foldback Current Limit

Current limit foldback can be implemented with the following components: R17, R18, C10, D5, and R16 (see *Figure 17*). At nominal output voltage (VOUT = 2.5V) D5 is reversed biased and the current limit threshold is still ~45mV. At lower output voltage the resistor divider network along with the forward biased diode (D5) will increase the voltage across R16. In order to reach the 45mV current limit threshold, the voltage across the sense resistor (R8) is reduced due to the increase in voltage across R16. Thus, the current limit is reduced providing current limit foldback. The resistor divider sets the voltage when current limit foldback kicks in and R16 sets the amount of current limit foldback.

Typical Performance Characteristics

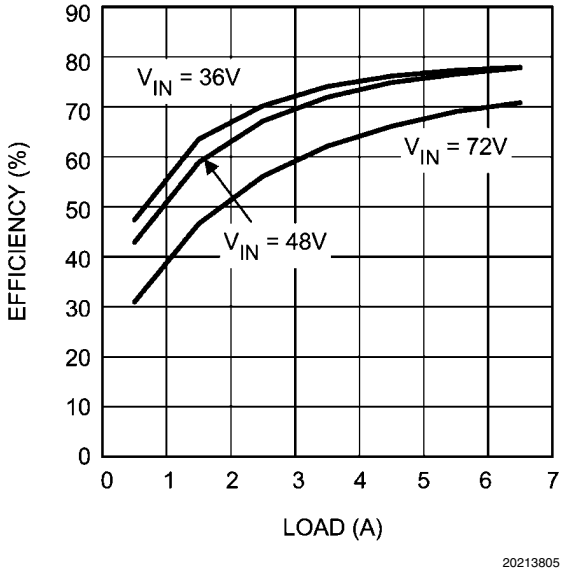


FIGURE 4. System Efficiency vs. Load Current and V_{IN}

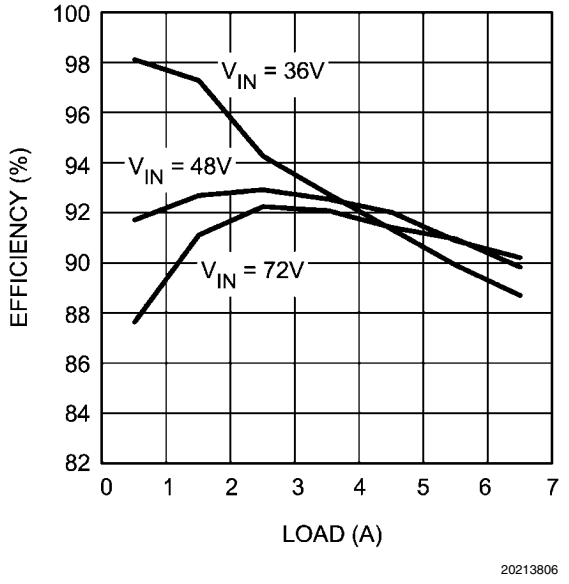


FIGURE 5. Adjusted Efficiency on secondary side vs. Load Current and V_{IN}

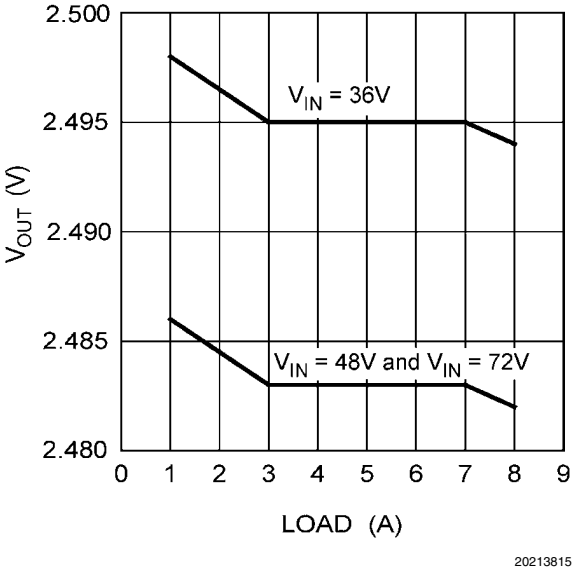


FIGURE 6. Output vs. Load Current & V_{IN}

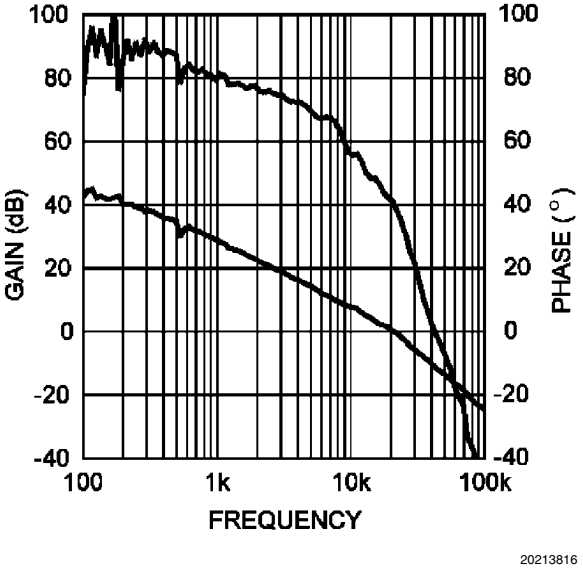
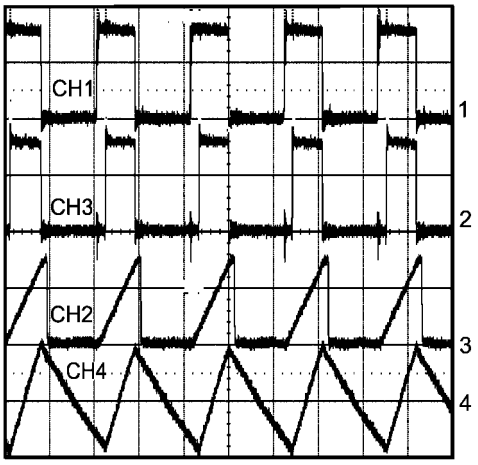


FIGURE 7. Secondary Closed Loop Frequency Response



V_{IN} = 48V, Secondary output load = open

CH1 = Main Phase Signal (5V/Div).
CH2 = RAMP (1V/Div).
CH3 = Secondary Switch Signal (5V/Div).
CH4 = Inductor Current Secondary (2A/Div).
Horizontal Resolution = 2 μs/Div.

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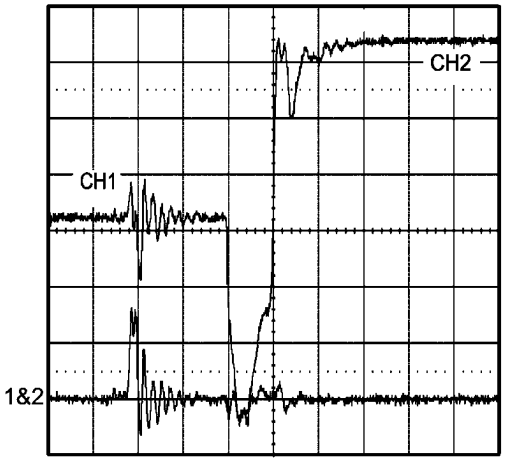
FIGURE 8. Representative Waveform



V_{IN} = 48V; LM5115 Load = 5.0A

CH1 = Lo Side Sw Gate Drive, 2V/Div.
CH2 = Hi Side Sw Gate Drive, 2V/Div.
Horizontal Resolution = 100 ns/Div.

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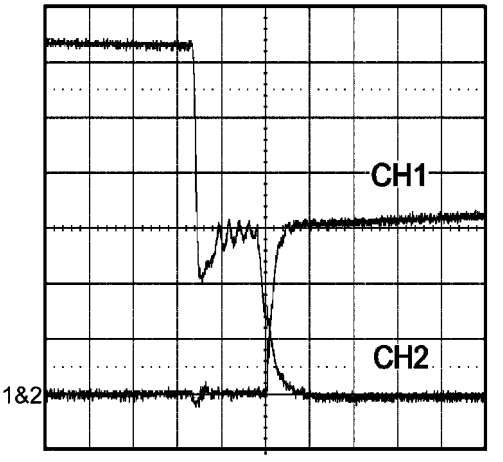
FIGURE 9. Gate Turn-on Delay



V_{IN} = 48V; LM5115 Load = 5.0A

CH1 = Lo Side Sw Gate Drive, 2V/Div.
CH2 = Hi Side Sw Gate Drive, 2V/Div.
Horizontal Resolution = 100 ns/Div.

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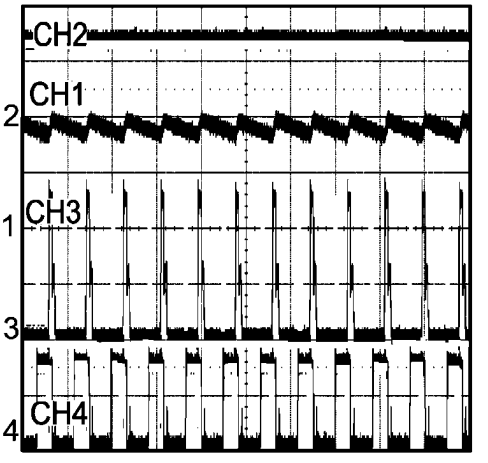
FIGURE 10. Gate Turn-off Delay



V_{IN} = 48V

CH1 = Inductor Current, 5A/Div.
CH2 = COMP/CO, 1V/Div.
CH3 = High Side Switch Gate Drive, 5V/Div.
CH4 = Phase Signal, 5V/Div.
Horizontal Resolution = 10 μs/Div.

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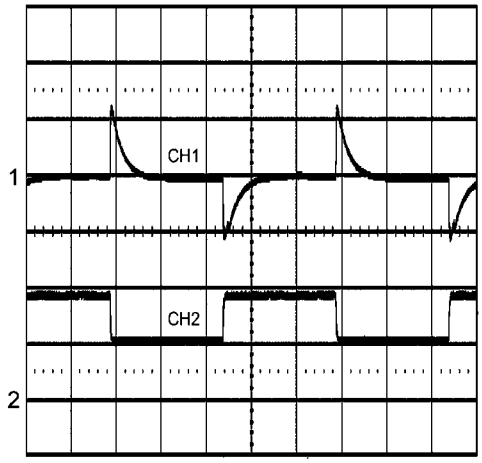
FIGURE 11. Secondary Output Short Response



V_{IN} = 48V
CH1 = Secondary 2.5V Output, 100 mV/Div, (AC Mode).
CH2 = Secondary Current Load (5A to 9A), 5A/Div.
Horizontal Resolution = 2 ms/Div

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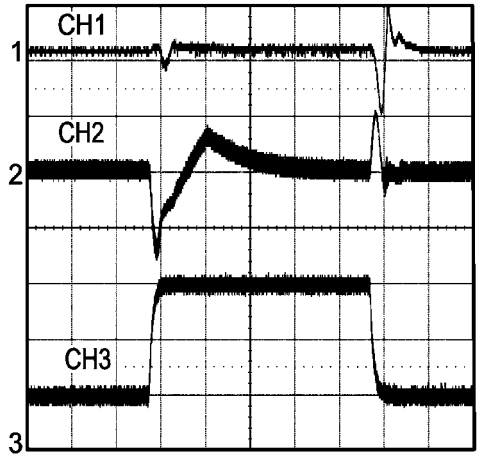
FIGURE 12. Secondary Step Load Response



V_{IN} = 48V
CH1 = Secondary 2.5V Output, 500 mV/Div. AC.
CH2 = Main 3.3V Output, 500 mV/Div.
CH3 = Main Current Load (10A to 30A), 10A/Div.
Horizontal Resolution = 200 μs/Div.

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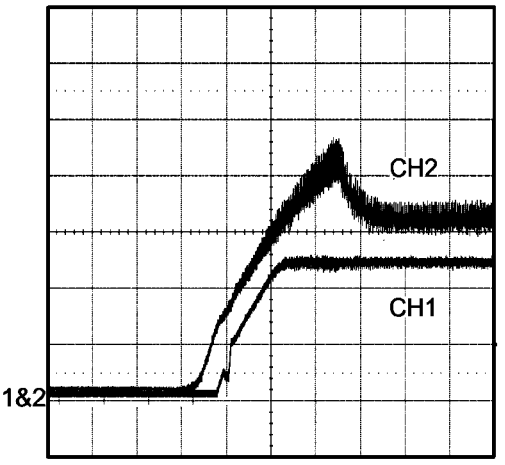
FIGURE 13. Cross Regulation Step Load



V_{IN} = 48V; LM5115A Load = 5.0A, LM5025 Load = Open
CH1 = Secondary 2.5V Output, 1V/Div.
CH2 = Main 3.3V Output, 1V/Div.
Horizontal Resolution = 500 μs/Div.

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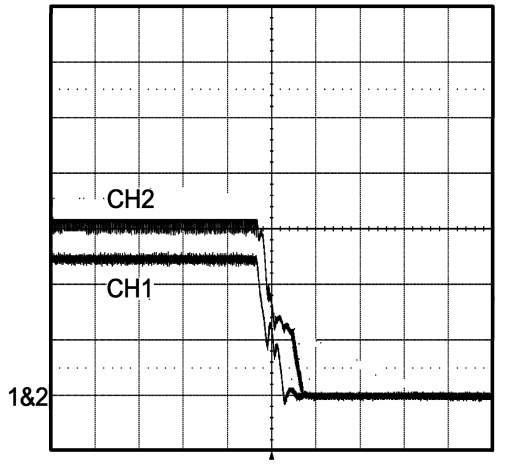
FIGURE 14. Startup Response



V_{IN} = 48V; LM5115A Load = 5.0A, LM5025 Load = Open
CH1 = Secondary 2.5V Output, 1V/Div.
CH2 = Main 3.3V Output, 1V/Div.
Horizontal Resolution = 200 μs/Div.

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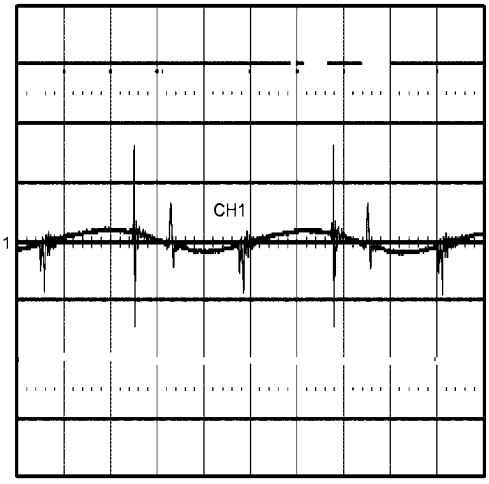
FIGURE 15. Shutdown Response

Output Ripple Measurement

Accurate Ripple and Noise measurements are difficult to obtain. The most accurate results are obtained when the measurement is taken as closely as possible to the converter's output terminals. Since the signal being measured is in the millivolt range and the measurement is made at a fairly high Bandwidth, the measurement setup can be susceptible to picking up noise from external sources and distorting the measurement results. The best way to minimize this effect is to use very short and direct connections to the oscilloscope probe such that the total loop area in the signal and ground connections is as small as possible. limiting the oscilloscope's bandwidth will also help.



V_{IN} = 48V; LM5115A Load = 8.0A
CH1 = Secondary 2.5V Output, 50 mV/Div. (AC Mode).
Horizontal Resolution = 1 µs/Div.

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FIGURE 16. Output Voltage Ripple

Application Circuit Schematic

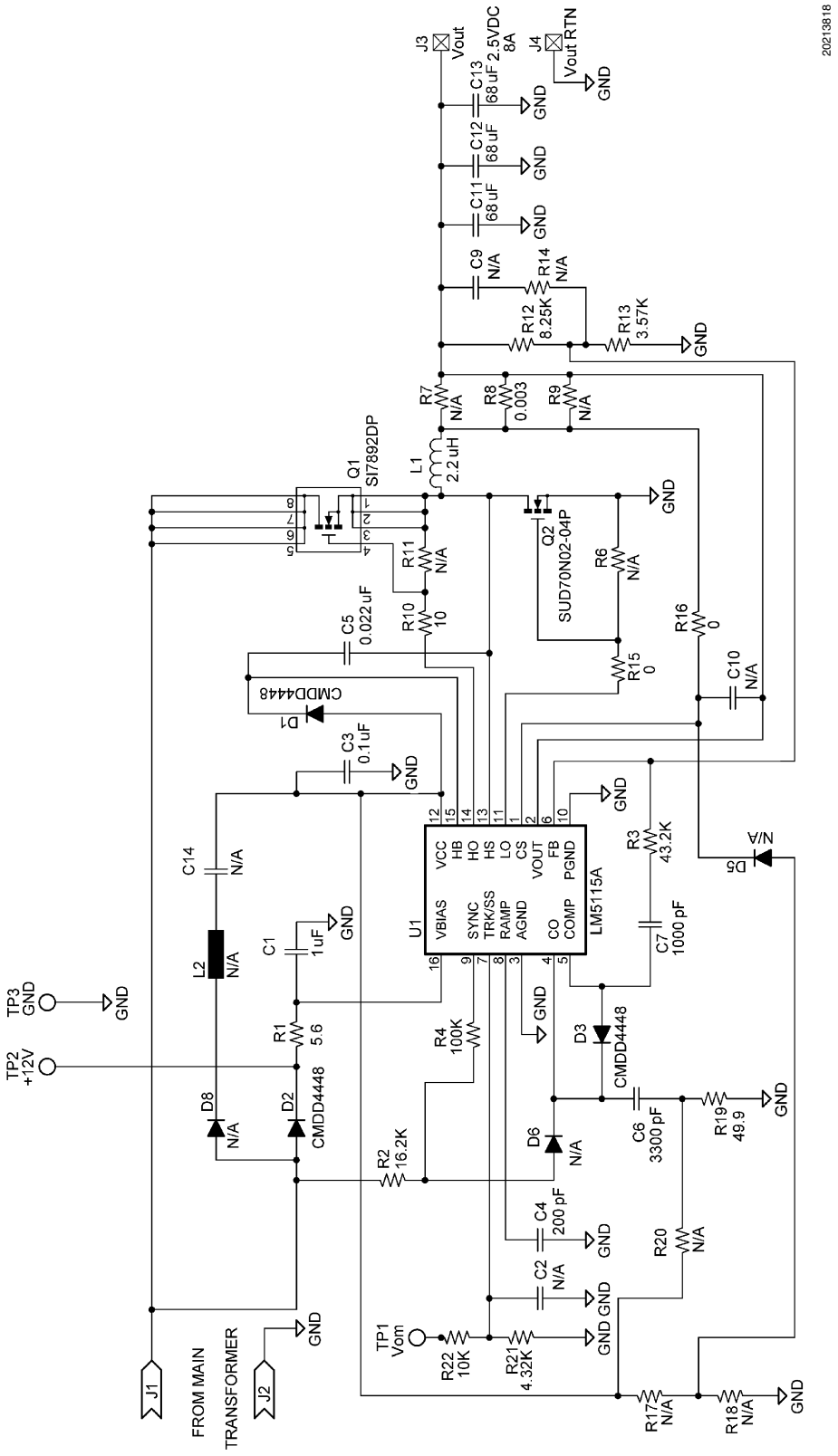

FIGURE 17. LM5115A AC Eval Board Schematic

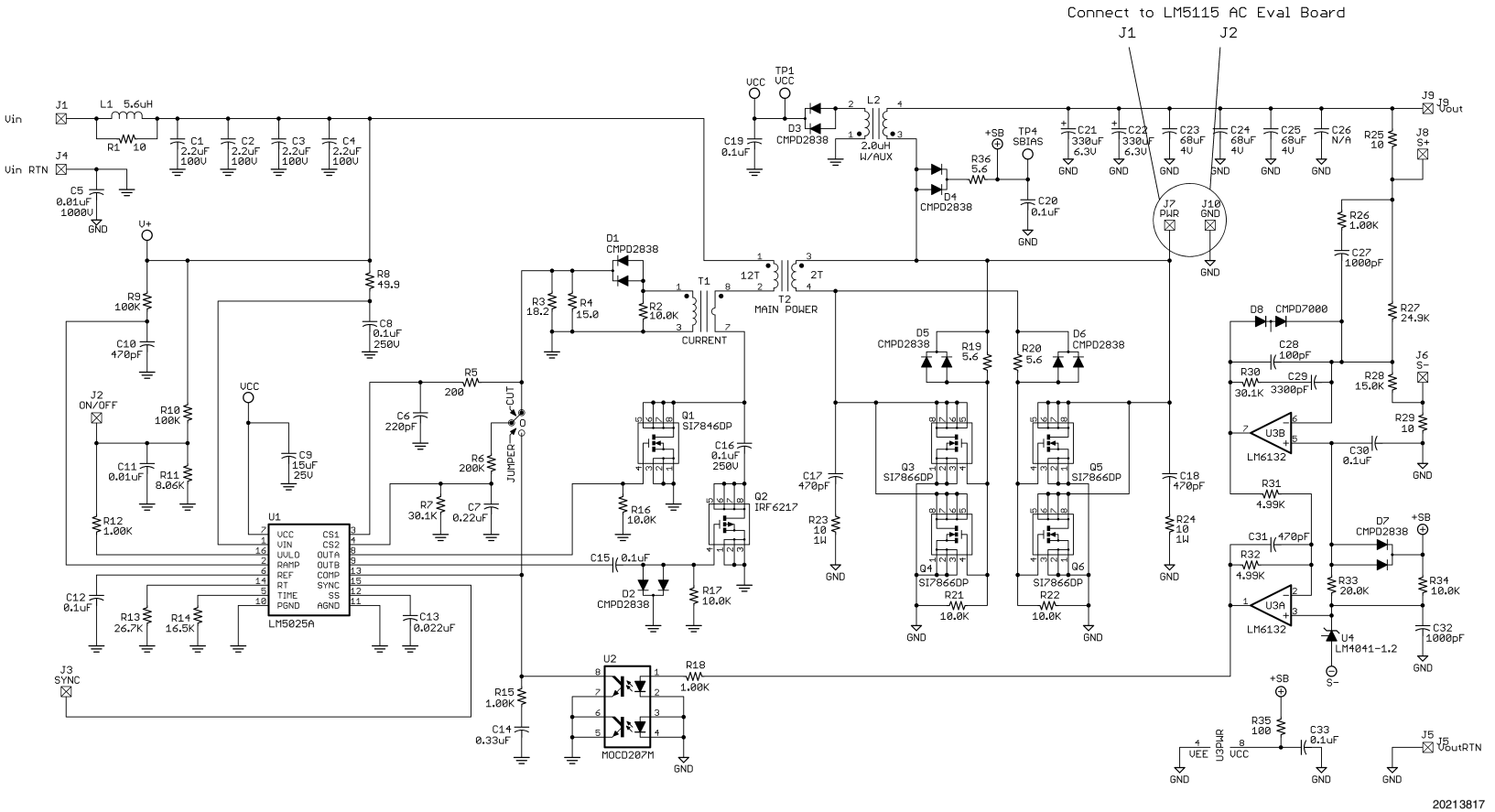

FIGURE 18. LM5025A Eval Board

Bill of Materials

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C3216X7R1E105K	CAPACITOR, CER, TDK	1.0 µF, 25V
C	2			Not Used
C	3	C3216X7R1E104K	CAPACITOR, CER, TDK	0.1 µF, 25V
C	4	C2012X7R1H201K	CAPACITOR, CER, TDK	200 pF, 50V
C	5	C2012X7R1H223K	CAPACITOR, CER, TDK	0.022 µF, 50V
C	6	C2012X7R1H332K	CAPACITOR, CER, TDK	3300 pF, 50V
C	7	C2012X7R1H103K	CAPACITOR, CER, TDK	0.01 µF, 50V
C	8			Not Used
C	9			Not Used
C	10			Not Used
C	11	C4532X7SOG686M	CAPACITOR, CER, TDK	68 µF, 4.0V
C	12	C4532X7SOG686M	CAPACITOR, CER, TDK	68 µF, 4.0V
C	13	C4532X7SOG686M	CAPACITOR, CER, TDK	68 µF, 4.0V
D	1	CMDD4448	DIODE, SIGNAL, CENTRAL, SEMI	
D	2	CMDD4448	DIODE, SIGNAL, CENTRAL, SEMI	
D	3	CMDD4448	DIODE, SIGNAL, CENTRAL, SEMI	
D	4			Not Used
D	5			Not Used
D	6			Not Used
D	7			Not Used
D	8			Not Used
J	1	2515-1-01-01-00-00-07-0	SOLDER TERMINAL SLOTTED, MILL-MAX	
J	2	2515-1-01-01-00-00-07-0	SOLDER TERMINAL SLOTTED, MILL-MAX	
J	3	5002	TERMINAL, SMALL TEST POINT, KEYSTONE	
J	4	5002	TERMINAL, SMALL TEST POINT, KEYSTONE	
R	1	ERJ-6RNF5R6V	RESISTOR, PANASONIC	5.6
R	2	ERJ-6ENF1622V	RESISTOR, PANASONIC	16.2 K
R	3	ERJ-6RNF4322V	RESISTOR, PANASONIC	43.2 K
R	4	ERJ-6RNF1003V	RESISTOR, PANASONIC	100 K
R	5			Not Used
R	6			Not Used
R	7			Not Used
R	8	WSL12063L000FEA	RESISTOR, VISHAY	0.003
R	9			Not Used
R	10	ERJ-6RNF10R0V	RESISTOR, PANASONIC	10
R	11			Not Used
R	12	ERJ-6RNF8251V	RESISTOR, PANASONIC	8.25 K
R	13	ERJ-6RNF3571V	RESISTOR, PANASONIC	3.57 K
R	14			Not Used
R	15	ERJ-6GEY0R00V	RESISTOR, PANASONIC	0 OHMS
R	16	ERJ-6GEY0R00V	RESISTOR, PANASONIC	0 OHMS
R	17			Not Used
R	18			Not Used
R	19	ERJ-6RNF49R9V	RESISTOR, PANASONIC	49.9
R	20			Not Used
R	21	ERJ-6RNF4321V	RESISTOR, PANASONIC	4.32 K
R	22	ERJ-6RNF1002V	RESISTOR, PANASONIC	10 K
Q	1	SI7892DP	MOSFET, N-CH, POWER S0-8 PKG, VISHAY	SI7892DP

ITEM		PART NUMBER	DESCRIPTION	VALUE
Q	2	IPD04N03LAG	MOSFET, N-CH, DPAK PKG, INFINEON	IPD04N03LAG
L	1	DR127-2R2-R	INDUCTOR, COOPER, DR127-2R2	2.2 uH - 12A
L	2			Not Used
TP	1	5012	TEST POINT, KEYSTONE	
TP	2	5012	TEST POINT, KEYSTONE	
TP	3	5012	TEST POINT, KEYSTONE	
U	1	LM5115A	CONTROLLER, SINGLE OUT, PWM, NATIONAL	LM 5115A

PCB Layout(s)

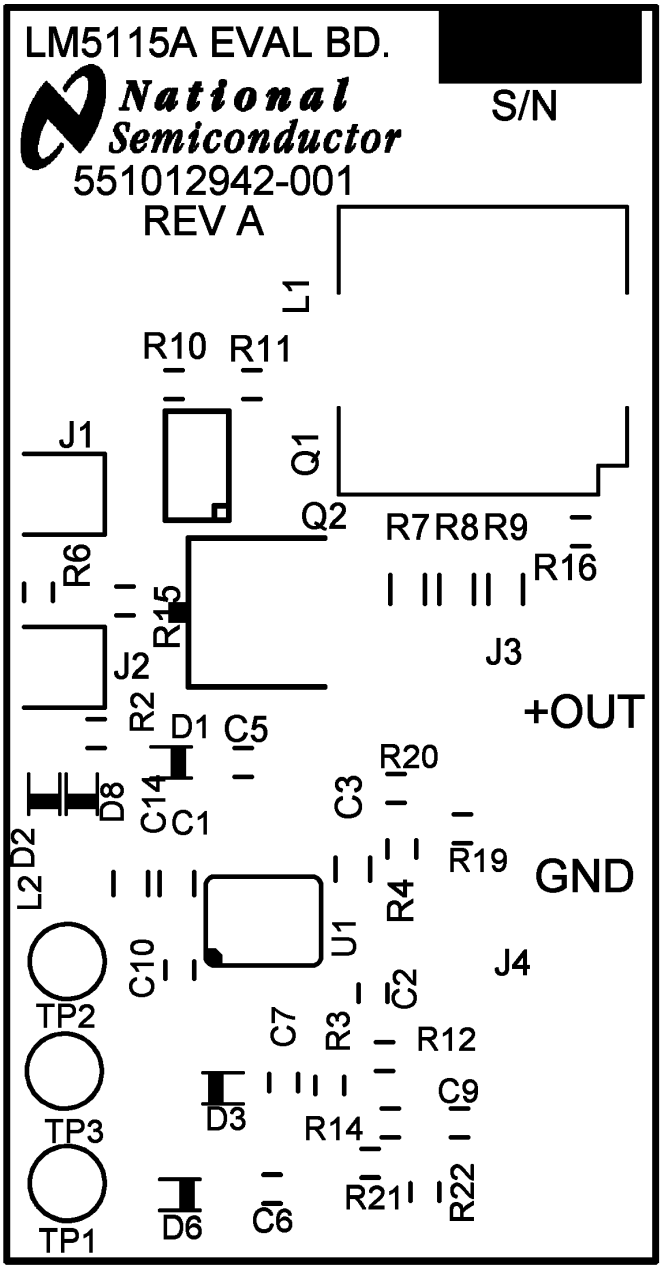

FIGURE 19. Top Silk Screen LM5115A

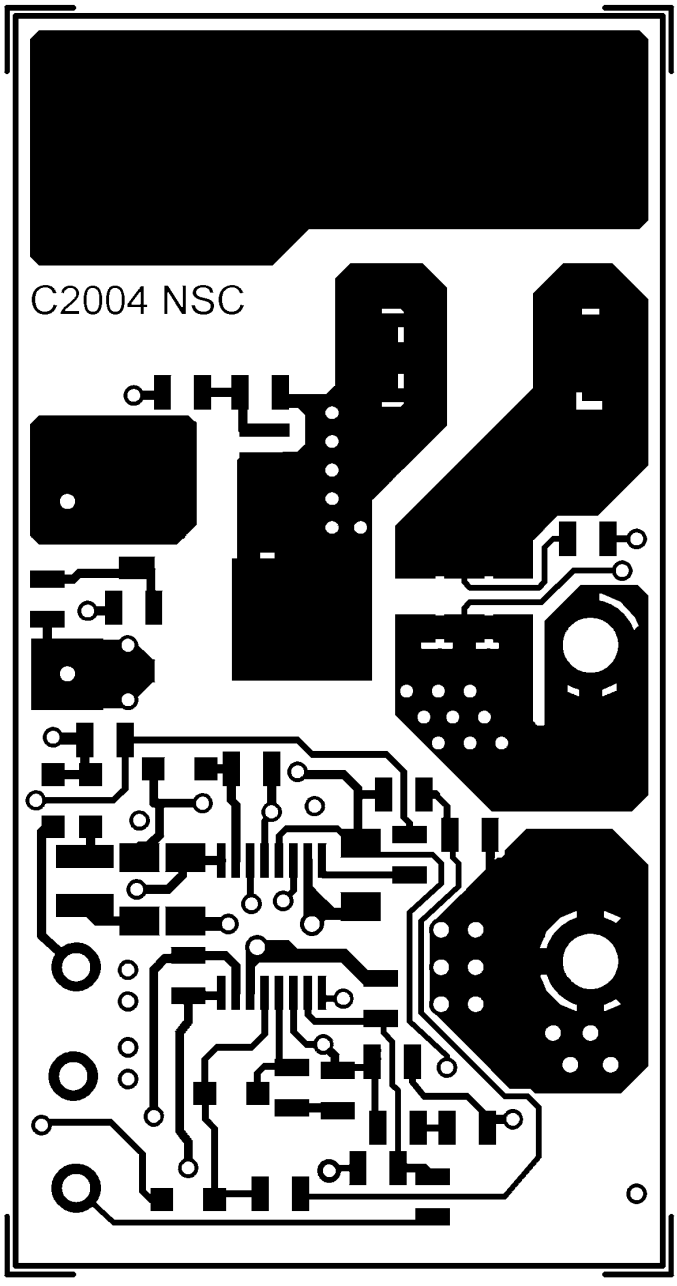

FIGURE 20. Top Layer LM5115A

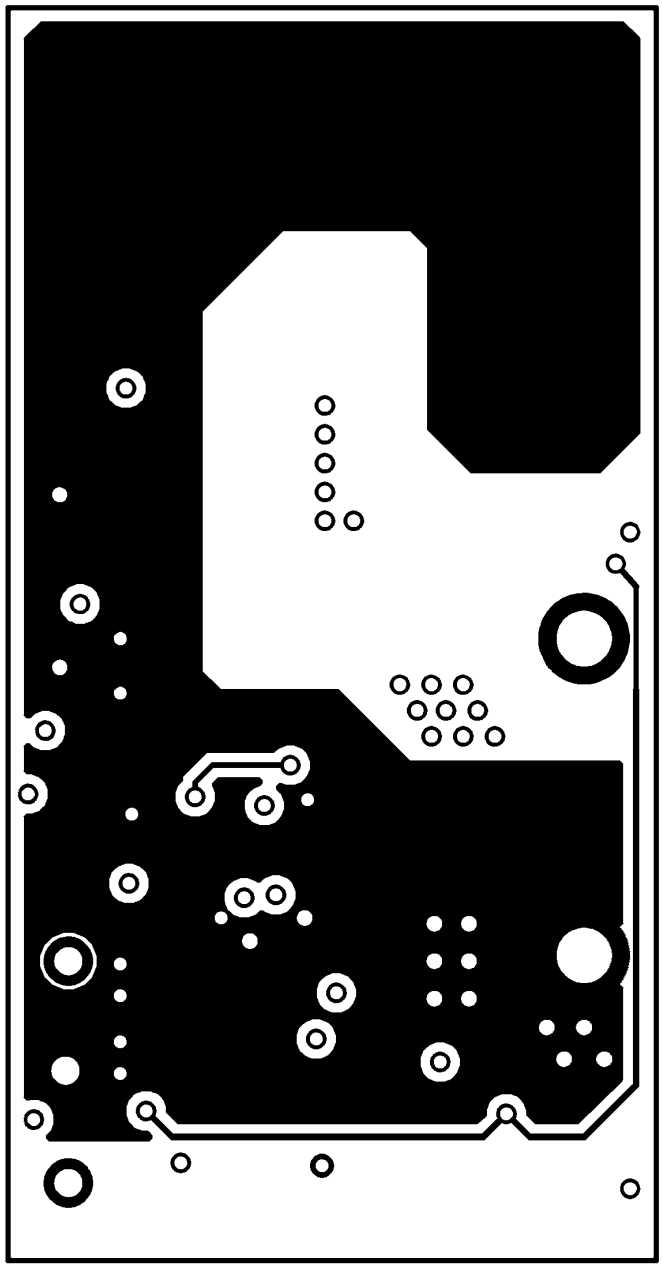

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FIGURE 21. Layer 2 LM5115A

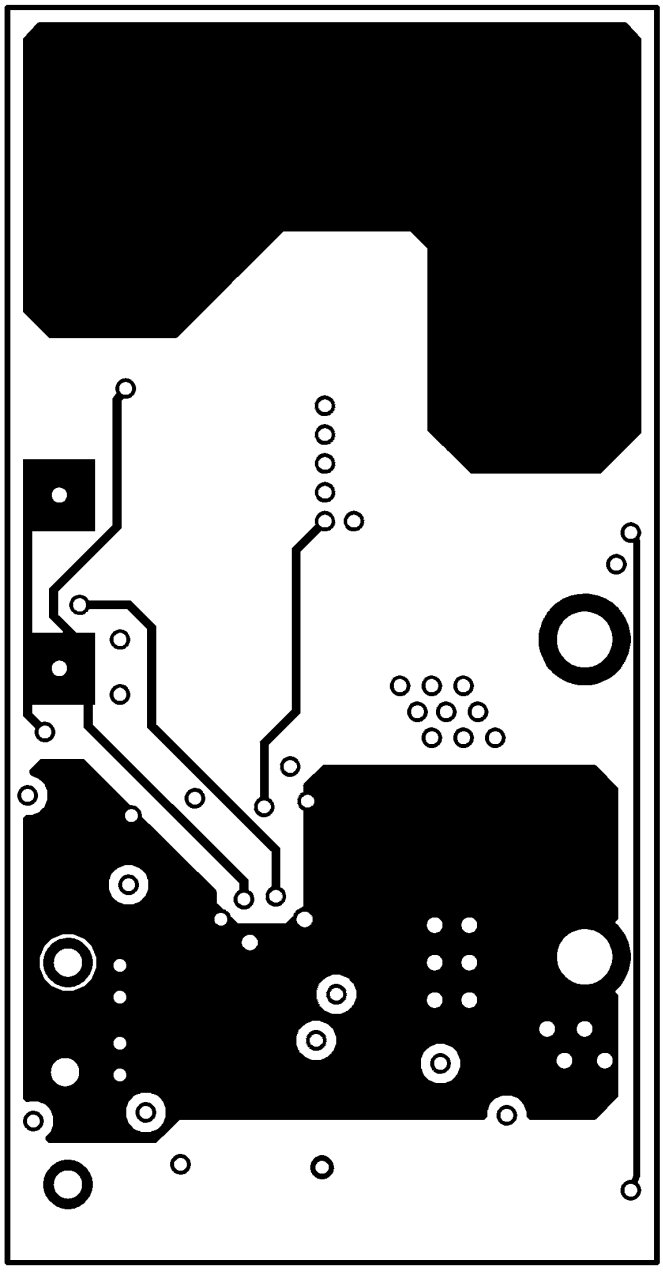

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FIGURE 22. Layer 3 LM5115A

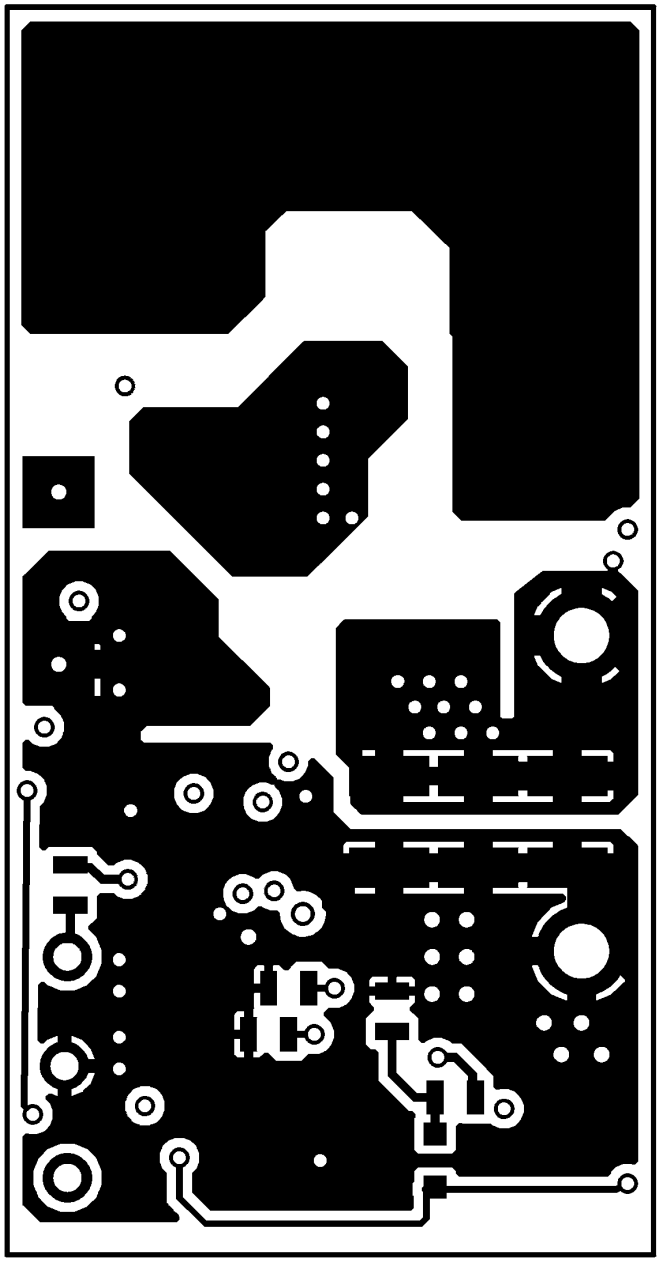

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FIGURE 23. Bottom Layer LM5115A, as Viewed from Top

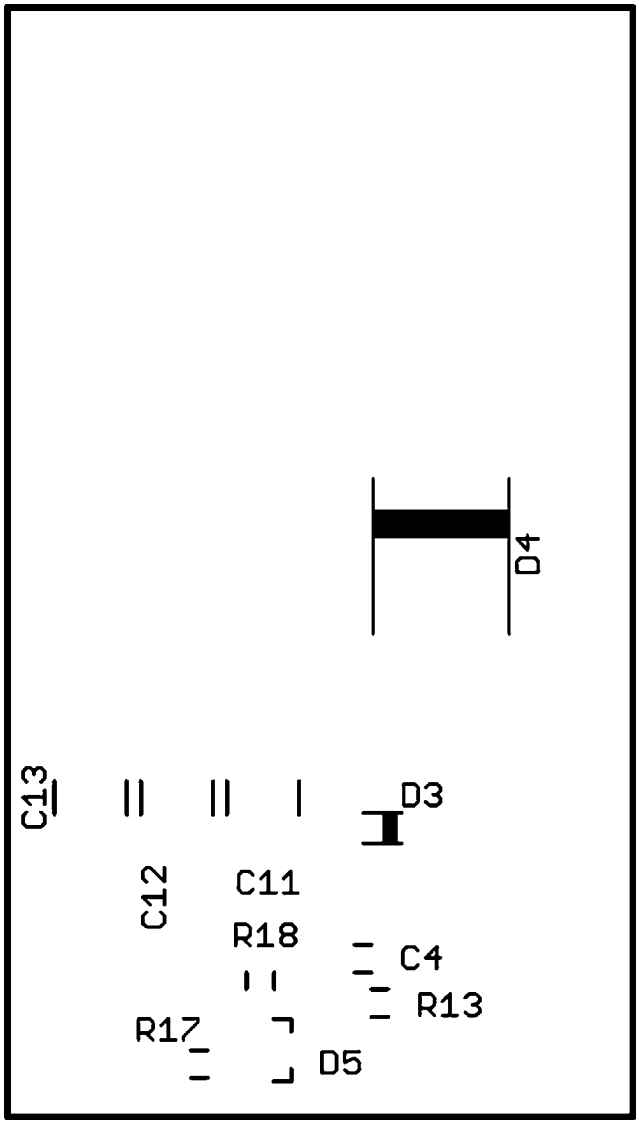

FIGURE 24. Bottom Silk Screen LM5115A

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